Abstract – In this paper is investigated the magnetic volume in a single-phase PFC boost converter with universal line input, taking into account the trade-offs between switching frequency, input current ripple and the generated differential mode noise, complying the IEC 61000-3-2 and CISPR 22 standards. The analysis is carried out considering that the boost inductor is built with a low-cost powder core material and with a single layer coil. This arrangement has been shown as a suitable layout for this application when constraints such as power density, leakage capacitances, irradiated noise and costs are taking into account. It is shown that an appropriate selection of the pair: switching frequency and input current ripple, during design procedure, can bring magnetic volume reduction when compared with the commonly adopted values for the mentioned variables.

1. INTRODUCTION

During the last years the world has observed a huge growth in the utilization the electronic equipments in industrial, commercial and household applications. These equipments need some kind of power conditioning, typically rectification, which produces a non-sinusoidal line current due to the nonlinear input characteristic. The cumulative effect of nonlinear loads is important, once the line current harmonics have a number of undesirable effects on both the distribution network and consumers. Therefore the compliance with international standards, such as IEC 61000-3-2 is a worldwide tendency. In this way, many power factor correction (PFC) ac-dc rectifiers to achieve high power factor and low total-harmonic distortion (THD) have been reported in the literature. For single-phase applications, the PFC boost converter operating in a continuous conduction mode (CCM) with the average current control method and universal line input is a well-known solution having a good acceptance for powers above 500W. A typical mass application is in DPS (Distributed Power Systems), where each module, in a power range of 1 to 2kW, needs a PFC converter in the front-end to comply with the standard aforementioned.

Nowadays, the design of a robust, reliable and low-cost PFC converter is one big challenge for power electronics engineers. Many technical papers and industrial reports have been published suggesting modifications in the typical PFC boost converter to mitigate its mains drawbacks.

Among its drawbacks, the most significant are the conduction losses, the commutation losses and the level of generated EMI noise. The conduction losses can be reduced by parallelism of main switch devices, by using newest power semiconductor devices such as CoolMOS [1] or by a topology modification that allow to reduce the number of series elements in the current path [2]. Concerning commutation losses, the major source of losses is the reverse recovery current of the boost diode, which can be minimized by using auxiliary commutation circuits, either active ones as passive ones [3], or by using the recent silicon carbide diode instead of silicon one [4]. On the other hand, to reduce the generated noise level, which can cause electromagnetic interference (EMI) in near equipments, several designs constrains must be obeyed in order to attain the compliance with EMI standards, such as the CISPR 22, which recommends maximum levels of conducted and irradiated noise for information’s technology equipments.

The earliest studies to achieve the compliance with EMI standards were based in a trial-and-error experimental approach made after design and breadboard stages. In the last decade, researchers and engineers have spent efforts in order to reduce the causes of the noise instead of blocking them [5]. The advantages of this approach are the reduction in the size, volume and cost of filters and shields, besides the reduction of the design and manufacture times. In order to illustrate this approach, the causes of common and differential mode noises are discussed in detail below.

The common mode noise is more related with leakages elements between the high dv/dt tracks of the board to the converter case [5, 6], while the differential mode noise is more affected by the switching ripple and the boost inductor leakage capacitance [7]. Therefore, the common mode noise generation can only be reduced by a layout modification, in such way that the leakages elements between the board and converter case are minimized. On the other hand, the differential mode can be reduced not only by reducing the leakages, but also by a design variable: the input current ripple. Therefore, there is a design trade-off among the input current ripple, the boost inductor size, the boost inductor leakages and the EMI filter size. Moreover, the switching frequency also has a considerable influence in the filter requirements, as shown in section II.A.

Another important aspect concerning the selection of the switching frequency and the input current ripple is the influence that these variables can causes in the total core losses. The volume reduction which is achieved with the increase of the switching frequency or current ripple can be lost when the core losses and temperature rise becomes excessive. The temperature rise of the core needs to be controlled to avoid the lost of its magnetic properties and permanent damaging. Therefore, the knowledge of the relationship among the switching frequency, the input current ripple and the temperature rise can contribute to establish an operation point that minimizes the boost inductor volume.

Aiming to define a procedure to estimate the boost inductor size, the interactions among the variables aforementioned are theoretically studied in [8]. However, the analysis is restricted to ferrite core as the magnetic material. Such arrangement has some drawbacks, as high leakage capacitances, low flux densities and irradiated noise generation in the concentrated gap. To avoid these problems, powder cores with a single layer winding layout are being widely adopted nowadays [5, 7]. However, this alternate array modifies the correlation between magnetic material volume and inductance, once that a single layer coil has a limited number of turns.

Therefore, this paper investigates the interactions among magnetic volume, switching frequency and the input current ripple considering that the boost inductor is assembled employing a cost-effective powder core material with a single layer winding layout. The objective is to bring improvements
on the magnetic volume by means of a careful selection of the mentioned variables. These improvements include higher power densities and lower cost, since the costs of the magnetic parts are meaningful in a PFC converter.

II. MAGNETIC ARRANGEMENT

Figure 1 shows the power elements of a single-phase PFC boost converter with the balanced PI-filter used as EMI filter. As can be seen, one end of the boost inductor is directly connected in a high dv/dt node, and therefore, any leakage capacitance will be able to reflect the high dv/dt variation as a high di/dt current in the input wires. These current spikes produce a high frequency noises that often are into the bandwidth of the EMI standard. Therefore, the leakage capacitance of the boost inductor plays an important role in the differential mode (DM) noise [7].

It is a good practice to use a winding layout that minimizes the leakage capacitance of the boost inductor, what is often done by the adoption of a single layer coil. Indirectly, this design procedure can help to minimize the size and costs of EMI filters, since it reduce the necessity of utilization of filter capacitors with low ESR and ESL, in order to block high frequency noise, and of filter inductor with special coil layout, for minimizing its own leakage capacitances.

Another advantage of single layer layout is a reduction in the losses caused by the proximity effect, which is highly dependent of the number of layers [9, 10]. As the single layer winding layout limits the number of turns by the magnetic material size, it is important to use a material that better fits this kind of coil. The powder cores in the toroidal shape can be a good choice, once that there are available low-cost models with high flux density and relative low core losses [11]. Besides, the use of distributed gap cores, such as powder cores, also contributes to mitigate the irradiated noise generated in the discrete gap of ferrite cores [11].

On the other hand, the restricted number of turns that a single layer winding demands enlarges the magnetic core volume for achieving a desired inductance, shifting the minimum points of the magnetic volume. In the next sections it is derived a methodology to find these new minimum points, considering the compliance with the international standards already mentioned.

Fig. 1. Boost Based PFC with a PI-type EMI Filter

III. DESIGN VARIABLES

Concerning a front-end PFC converter, the output capacitor generally is chosen to meet a given hold-up time specifications and, consequently, its size can not be optimized. Therefore, the main motivation for increasing the switching frequency and/or the input current ripple amplitude is to obtain a possible reduction in the boost inductor volume.

Soft saturation powder cores are being widely used in this application due to its significant design advantages, such as: a) higher flux densities capabilities which result in smaller size; b) minor sensitivity to variation in its magnetization curve, either due to temperature or material tolerances; c) natural fault tolerance; d) natural swinging inductance – high L at low load, controlled L at high load; e) less susceptible to fringing losses and gap EMI effects. However, these materials present higher AC losses than ferrite types [11].

It is well known that in all magnetic cores, the operation temperature needs to be controlled in order to retain its magnetic properties and limit the losses. The switching frequency and input current ripple values have important influence in such losses. Therefore, there are values of the switching frequency and input current ripple where the advantage of the inductor volume reduction is lost, due to the excessive temperature rise. As the soft saturation powder cores produce higher AC losses than ferrite cores, the influence of these design variables must be known in order to achieve the mentioned advantages.

Furthermore, the switching frequency also has effect on the commutation losses and on the EMI filter requirements. The current ripple also has effect on the commutation losses, on the conduction losses and on the EMI filter requirements. A higher ripple tends to increase the RMS current in the main switch, and hence, can increase the conduction losses if a MOSFET is being used. Concerning commutation losses, a higher input current ripple will produce higher turn-off losses and smaller turn-on losses [12]. Hence, the influence of the input current ripple in the commutation losses only can be predicted if a deep analysis about the semiconductor technology utilized is considered, once the commutation losses can be significantly different depending on it.

Nevertheless, if new semiconductors technologies are employed, such as the CoolMOS Power MOSFET and the Silicon Carbide Diode (SiC), the switching losses are drastically reduced. In such case, for switching frequencies as high as 400kHz, the most responsible for the heat sink volume in a 1kW PFC are the conduction losses [13, 14]. Therefore, in this paper the effect of the switching frequency and current ripple on the heat sink volume will not be considered, once the use of aforementioned newest semiconductors technologies will be a worldwide tendency with the decrease of its cost. Hence, in such conditions, the most affected parts in a boost PFC converter are the boost inductor size and the EMI filter size.

On the other hand, the influence of switching frequency and input current ripple in the generated DM noise, which will dictate the EMI filter attenuation requirements, is a bit more complex and is discussed in detail in the next topics.

A. Switching Frequency versus DM-Noise

In this analysis the switching frequency is considered constant, what makes the spectra be composed of discrete harmonics that are integer multiples of that frequency. As the CISPR 22 standard limits the noise amplitude only above 150kHz, any harmonic component below of this value can be ignored. On the other hand, the first harmonic of the spectra above 150 kHz, in most cases, will dictate the required EMI filter attenuation [15]. This is due to the fact that the filter attenuation slope is more accentuated that the standard limit slope. Therefore, in theory, it means that if the lowest critical harmonic is conformed, all harmonics of superior order will be also confirmed.

To illustrate, Figure 2 shows of the conducted noise obtained by a Fast Fourier Transformer routine in a simulation of the single-phase PFC boost converter, operating in 70 kHz, with an EMI filter that matches the attenuation requirements. It is possible to see that only from 3ª harmonic to the fore, the harmonic spectrum is within of the frequency range of the CISPR 22 standard (150 kHz – 30 MHz). Thus, in this case, the
3rd harmonic is called the “critical harmonic”. Another consequence of the slope differences between the filter attenuation and standard limit is that as higher the critical harmonic frequency is, lower will be the required attenuation. Therefore, the switching frequency is higher than 150kHz, the first harmonic is inside the standard limited bandwidth, hence, as higher the switching frequency is, higher will be the filter attenuation. However, only at switching frequency higher than 400kHz the attenuation requirements reach a comparable magnitude with those cases that use frequencies below 150kHz [13].

An important point that needs to be considered when the switching frequency is chosen is the 9kHz bandwidth utilized in the quasi-peak detector measure, specified in the measurement methods standard (CISPR 16). Thus, if a switching frequency below 150kHz is selected, any harmonic within the region given by (150±4.5)kHz contributes for the quasi-peak measurement at 150kHz, the beginning of the CISPR 22 limited region. As a result, only switching frequencies that produce a harmonic slight below 145.5kHz should be used to minimize the filter requirements. Adding a further safety margin to prevent frequency variations from actual oscillators, one can select sub-multiples of 140kHz as a reasonable choice.

In a front-end PFC converter, usually the EMI input filter utilized is the balanced PI-type as shown in Figure 1. In such filter, the DM noise is attenuated by de $C_{DM}$ capacitors and by the $L_{DM}$ inductors. The value of the $C_{DM}$ capacitors are limited by the displacement factor of the input current, and the $L_{DM}$ inductors are frequently the leakages inductances from the $L_{CM}$. Therefore, the DM attenuation level of the filter will depend of the CM attenuation level, and when a given filter is correctly designed to block the CM noise, a certain DM attenuation capability becomes automatically defined. As changes in the input ripple amplitude have small influence in the CM noise, the input current ripple can be increased up to the DM attenuation capabilities of the designed filter.

**IV. SIMULATION ALGORITHM AND RESULTS**

The proposed simulation algorithm is a new approach that is able to estimate the minimum single layer core size based either in the core energy storage capability as in the maximum temperature rise, caused by the total core losses. However, it is important to highlight that all utilized models in the algorithm already were tested and confirmed in the literature [11, 18, 19]. Therefore, the objective of proposed simulation algorithm is determine the minimum boost inductor size for a vector of input current ripple amplitude values and for several switching frequencies obeying the restriction mentioned in section III.A. In this way the following guidelines were used:

1. The chosen magnetic material was a ferrous alloy material (Fe-Si-Al) known as Sendust toroidal core shape. For PFC applications, the Sendust cores present a very good commitment between cost and performance when compared with another soft saturation magnetic materials [11]. Form-factors were considered based in the commercial Sendust cores dimensions, with the relationship shown in (1) and (2), in such way that all the geometrical variables of the core can be calculated using its outside diameter, and the form factors values. With this arrangement the outside diameter can be changed in a continuous fashion until the algorithm finds the minimum core size for the selected operation conditions. After that, the next higher commercial core could be selected for implementation on the actual case:

\[
k_f = \frac{OD}{ID} \quad (1)\]

\[
k_h = \frac{H}{OD-ID} \quad (2)\]

Where:
- $k_f$: thickness form factor;
- $k_h$: height form factor;
- $OD$: core outside diameter;
- $ID$: core inside diameter;
- $H$: core height;

2. The selection of the core permeability is done following the chart method recommended by [20], which assumes a permeability reduction of no more than 50% with the maximum DC bias. It consists in the calculation of the value: $L_{DC}^2$, with a consecutive selection of the recommended core permeability through the chart.

3. The winding arrangement considered is single layer. A 0.95 winding factor is assumed relative to the maximum single layer number of turns, as shown in (3). In case of the required number of turns be smaller than the maximum
feasible for the considered core, the wire diameter \((d_w)\) is enlarged until the coil fills 95% the available space. A minimum wire diameter is set based in a maximum current density of 600A/cm²:

\[
N_{\text{max}} = 0.95 \pi \left( \frac{OD}{d_w} \right) - 1
\]  

(3)

4. The design and the simulation of the single-phase PFC boost converter with universal line input voltage is done for the worst case, that is, the minimum input voltage and the estimated efficiency which produces the highest input current.

5. The input current ripple amplitude is expressed in a percentage of the maximum sine input current [17]. It is calculated in peak-to-peak for the peak of the minimum input voltage as mentioned above. Moreover, as mentioned in the item 2, it is important to consider the powder cores inductance variation. Therefore, the ripple must be obtained for the inductance value that happens in the considered instant of calculus. For the peak of sinusoidal input current, the minimum inductance value needs to be used.

\[
\text{Ripple(\%)} = 100 \frac{|\Delta i_{\text{line-peak}}|}{I_{\text{line-peak}}} \frac{V_{\text{in of Low Line}}}{V_{\text{out}}}
\]  

(4)

\[
\Delta i = \frac{V_{\text{line-peak}}D_{\text{max}}}{L_{\text{min}}} f_s, \quad D_{\text{max}} = 1 - \frac{V_{\text{line-peak}}}{V_{\text{out}}}
\]  

(5)

Where:

- \(V_{\text{line-peak}}\): Peak of minimum RMS input voltage;
- \(D_{\text{max}}\): Minimum duty cycle;
- \(L_{\text{min}}\): Minimum inductance of boost inductor;
- \(f_s\): Switching frequency;

The Figure 3 contains a simplified flowchart of the simulation program, which was developed using the Matlab® software. For each switching frequency and input current ripple pair, it is calculated the minimum core that satisfy the inductance requirements and that be outside the saturable region. Then, the obtained core is simulated in the specified conditions to obtain its losses, the copper losses, and finally, the temperature rise. In case of the temperature rise be greater than the specified value, the core is enlarged in a small percentages until the temperature rise be inside a tolerable range.

To simulate the operation of the core in the PFC a discrete model of boost converter was utilized, what uses a PI compensator to control the input current envelop. The simulation step was chosen to produce a Nyquist frequency of 15MHz, what is enough to represent with good precision signals up to 1.5MHz.

A. Core Losses Model

The core losses are calculated using the method derived in [18], where the duty cycle variations are automatically considered. This feature is crucial on the PFC case. In this method the losses are calculated at each commutation cycle, through the stored values of magnetic flux variations, \(t_{\text{on}}\) and \(t_{\text{off}}\) times, as defined in (6).

\[
P = \alpha \frac{\Delta B^\pi - \Delta B^\mu}{2t_{\text{on}}} t_{\text{on}} + \frac{\Delta B^\mu}{2t_{\text{off}}} t_{\text{off}}
\]  

(6)

Where:

- \(P\): Core losses;
- \(V\): Core volume;
- \(a, m, n\): Steinmetz equation coefficients;
- \(T_s\): Switching period;

The recommended Steinmetz coefficients to be used are those taken from a square wave excitation of the core. However, in general, the manufactures does not provide such coefficients or curves, but only that resultant from sine wave excitation. Fortunately, the losses with sine wave excitation are just slight higher than that from square wave excitation in powder cores [21]. Therefore, the sine wave coefficients are used in (6) which can be considered as a conservative approach.

As a particularity of the soft saturation materials [13], the inductance variations as a function of the core magnetization are take into account to estimate with accuracy the core losses and DM noise. To accomplish this task the inductance value of the boost inductor is constantly updated during the simulation, using a fitting equation of the DC magnetization curve versus the permeability reduction, which is provided in [20].

Figure 4 contains the input current waveform resulted from a simulation of the discrete model of the single-phase PFC boost converter operating in the continuous current mode. It can be seen that the switching current slope contains a curvature due to the soft saturation effect. This simulation was done for a switching frequency of 70kHz, 1.1kW input power, 400V output voltage and at a maximum input current ripple of 55%.

Fig. 4. Input current from the discrete model simulation.

B. Copper Losses Model

The copper losses are calculated considering the copper resistivity and the RMS current obtained in the simulation, since it depends on the input current ripple. The proximity effect is not considered, once the inductor employs a single layer coil, what significantly reduce this effect [9, 10]. The skin effect can also be neglected due the fact that the most significant current harmonic is low order, it is, the rectified input line frequency (100/120Hz). The harmonics starting from the switching frequency and higher have a much smaller
amplitude, and therefore, its influence in the total copper losses has much less impact.

C. Temperature Rise Model

The temperature rise calculus is based on an empirical equation [20], what is shown in (7). It is based on the total surface area for the heat transfer and in the total losses for the wound core.

\[
\Delta T = \left( \frac{(\text{Core Loss} + \text{Copper Loss})}{\text{Surface Area}} \right)^{0.833} \text{[°C]} \quad (7)
\]

It is important to mention that it is not an easy task to define the maximum allowable temperature rise, once it has a strong dependence with some operating conditions, such as airflow and temperature inside the equipment case. In the case of the Sendust cores, they can operate up to 200°C, but such magnitude can be harmful to the board, to near components and also can reduce the core lifetime [22]. Selecting 100°C as reasonable maximum core temperature, regarding the mentioned restrictions, it is possible to allow a temperature rise of 50°C, once that the temperature inside the equipment case can be as high as 50°C. It is clear that others values for the maximum temperature rise could be used and it is a designer task based on the rule of thumb, considering its specific case.

D. Simulation Results

The simulation of the single-phase PFC boost converter with universal line input voltage was done with the proposed algorithm to find the minimum boost inductor volume, considering the mentioned trade-offs between switching frequency, input current ripple and the core losses. It was considered in this simulation example, an output power of 1kW, an output voltage of 400V, a minimum input voltage of 90V$_{RMS}$ and a minimum efficiency of 90%. The Sendust core adopted in the simulation was a Kool Mu$^\text{®}$ cores from Magnetics$^\text{®}$. It was considered 2 stacked toroidal cores to settle the final core size within the commercial range. The adopted staking configuration is adjusted on the simulation program by the $k_s$ form factor, which is multiplied by the number of stacked cores.

Figure 5 shows the total boost inductor volume as a function of the switching frequency and input current ripple values obtained by the simulation. The switching frequencies used are chosen following the restriction imposed in section III.A in order to minimize the required attenuation to reach compliance with the EMI standard. The input current ripple was varied from 10% to 70%, and the percentage value is calculated by equation (4). The volume measurement is relative to the material amount, i.e., the toroidal center hole is not enclosed, since this result tends to be more related with the final magnetic costs.

The analysis of the Fig. 5 elucidate that when a temperature rise restriction is considered, the switching frequency elevation does not deliver all its supposed benefits. The minimum volume of the 46.6kHz curve happen at about a 70% ripple. Taking the 46.6kHz curve as a reference, the minimum volume of the 70kHz curve saves about 13% of volume, the 140kHz curve saves about 29% and the 400kHz curve saves 47%. It is important to note that the highest frequency is more than eight times higher than the smallest frequency, while the volume reduction does not reach a half part from one case to another.

Moreover, besides the comparison of different switching frequencies, the Fig. 5 reveals the input current ripple magnitude that minimizes the inductor volume for each switching frequency, which can be significantly different from one frequency to another, and also is dependent of the selected maximum temperature rise and input power.

Nevertheless, as the input current ripple amplitude affect the DM noise, it is necessary to check if the input current ripple that minimizes the inductor volume will not produce excessive noise to comply with the EMI standard. Hence, the quasi-peak value of the critical harmonic, for each simulated point, was estimated using the method derived in [19]. As the critical harmonic is different for each switching frequency, the comparison is carried out using the necessary filter’s cutoff frequency to achieve compliance with the CISPR 22 standard. The cutoff frequency here considered is the point where the filter’s slope asymptote crosses the unitary gain axis. Figure 6 contains the results of this analysis, which includes a 3dBµV safety margin. A line in 9kHz is highlighted to represent a typical cutoff frequency, extracted from the DM filter parameters used in [6], which also uses a balanced PI filter on a similar base line.

**Fig. 5.** Boost Inductor Volume (i.e. core volume plus copper volume) versus Input current ripple amplitude for 4 switching frequencies

**Fig. 6.** Maximum DM Filter’s Cutoff Frequency to Comply with CISPR 22 Standard

Figure 6 shows that, for the considered one stage PI filter and input current ripple range, the DM-noise is not the most imperative restriction regarding the input current ripple amplitude elevation. Theoretically, in all cases the considered filter is able to leads to compliance with the CISPR 22 standard in the low frequency range (150kHz – 1MHz), for the ripple points where the minimum volume is achieved. However, in the actual case a further safety margin can be necessary to prevent the effects of non-modeled elements as well as to prevent the

![Fig. 5. Boost Inductor Volume (i.e. core volume plus copper volume) versus Input current ripple amplitude for 4 switching frequencies](image)

![Fig. 6. Maximum DM Filter’s Cutoff Frequency to Comply with CISPR 22 Standard](image)
PFC input voltage variation, which changes the input current ripple waveform shape.

Furthermore, it is important to know the influence of high input current ripple amplitude in the main switch conduction losses when a MOSFET is used. Therefore, the main switch RMS current was computed in the simulation algorithm, and the results are plotted in the Fig. 7. It can be seen that, for the considered input current ripple range and worst case of input voltage, the RMS switch current does not modify significantly, and therefore, such variation can be neglected. Only the 70kHz case is shown since the other ones are very similar.

The simulation results confirm that the adequate selection of the switching frequency and of the input current ripple can brings effective reduction for the boost inductor volume in PFC boost converters when a maximum core temperature rise is considered. For the simulated PFC base line, considering a maximum core temperature rise of 50°C, the minimum boost inductor volume is obtained for the following values of the switching frequency and of the input current ripple: A)46.6kHz and 70%; B)70kHz and 55%; C)140kHz and 35% or D)400kHz and 15%. The choice of what case should be used can be done pondering the switching losses augment with the boost inductor size reduction. It is well known that the switching losses are proportional to the switching frequency, which means losses about three times higher from option A to C, and more than eight times higher from A to D. However, the inductor volume saved does not exceed 47% for the extreme cases.

The variables that could be analyzed at this point are the converter efficiency and the required heat sink size. However, as commented in section III, to proceed to this analysis is necessary the definition of the set of semiconductors technologies that intended to be used. If the choose semiconductor set employs a CoolMOS as power switch and a SiC diode as boost diode, the prototype could be designed for the operation points C and D. However, it is highlighted that the point C can provide higher converter efficiency, while the converter volume could be virtually the same at both points. It is important to consider that the gain obtained by the inductor volume reduction in the operation point D can be easily lost by the heat sink size increasing due to the significantly higher switching frequency. On the other hand, it is well known that the use of majority carrier devices (MOSFET), which has a resistive behavior when in its “on” state, leads to a high conduction loss on the 1kW PFC due to the elevated current levels, even in the CoolMOS case [14]. This fact can demand the use of paralleled devices to control the conduction losses and to prevent thermal run-away. An alternative choice can be the use of a minority carrier device (IGBT) once a single switch can be enough to limit the conduction loss. However, if the switch choice is an IGBT, even those designed for higher switching frequency, the operation points A and B must be considered. The reduction of the conduction losses may balance its higher switching losses and higher boost inductor volume, however, the final result is dependent of many variables and can not be predicted without a deep analysis, what is out of the scope of this paper.

In [14], it was made a comparison of a 100kHz PFC using well established semiconductor technologies with a 400kHz PFC using the newest semiconductor technologies. It is reported that the efficiency is practically the same in both cases, and concerning the boost inductor size, a footprint reduction of 60% was achieved pushing the switching frequency to 400kHz. A simulation for a 100kHz core operation in the algorithm here developed show a minimum volume of 29cm³, at the input current ripple of 45%, while the 400kHz case achieve 20cm³ at 15%. About 31% of reduction on the volume is verified as a result of a four times higher switching frequency. Unfortunately, the results can’t be directly compared once the footprint may not represent the inductor volume, since it depends on the core diameter. Moreover, in [15], it was not informed the final core temperature rise of each case, that is, 100kHz and 400kHz PFCs. Regarding the EMI filter requirements, the comparison between these PFCs approaches tends to be unfair, once the switching frequency of 100kHz does not minimize the filter attenuation requirements when the CISPR 22 standard is applicable. As explained in section III.A, a switching frequency of 70kHz or 140kHz should be used instead for this comparison purpose.

V. EXPERIMENTAL RESULTS

To evaluate the core temperature rise estimation made by the proposed simulation algorithm, a 500W (400V, 1.25A) universal line input (90-264 V_{RMS}) PFC prototype was implemented considering a switching frequency of 140 kHz. For these specifications and a maximum temperature rise of 50°C, the simulation algorithm indicates a minimum boost inductor volume at an input current ripple of about 45%. It is highlighted that this point differs from to that shown in Fig. 5, due to the output power difference. The real core utilized was the Kool Mu part number 77083, which allow the use of an input current of 45%, while the 400kHz case achieve 20cm³ at 15%. About 31% of reduction on the volume is verified as a result of a four times higher switching frequency. It is highlighted that this point differs from to that shown in Fig. 5, due to the output power difference. The real core utilized was the Kool Mu part number 77083, which allow the use of a single core instead the stacking option in this case. The maximum number of turns was 52 with the AWG 16 wire size, and the verified current ripple for such configuration was 46.5%. The inductance value swing from 232µH, when at a near to zero magnetization current, to 166µH when at the maximum input current, i.e., at the peak of the sinusoidal input current.

Two operation points were tested, which are described in the Table 1. Although the oscillator components of the control integrated circuit have been calculated for 140 kHz, the verified actual switching frequency was of 147 kHz, after one hour of operation. The temperature was measured with a thermocouple inserted in a small hole made in the core, as suggested in [23].

An another simulation using the real conditions measured in the practice for each case, regarding switching frequency, input power and input voltage, yields a temperature rise of 43.3°C for the full load case and 34.3°C for the partial load case. An error of 2.3°C and 4.3°C is verified for the full and partial load cases respectively.

| Table 1. Experimental prototype conditions and results |

<table>
<thead>
<tr>
<th>Variable \ Load</th>
<th>Full Load</th>
<th>Partial Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMS input voltage</td>
<td>90V</td>
<td>90V</td>
</tr>
<tr>
<td>Actual Input Power</td>
<td>500W</td>
<td>178W</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>27°C</td>
<td>27°C</td>
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<tr>
<td>Final Measured Temperature</td>
<td>68°C</td>
<td>57°C</td>
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<tr>
<td>Experimental Temperature Rise</td>
<td>41°C</td>
<td>30°C</td>
</tr>
<tr>
<td>Simulated Temperature Rise</td>
<td>43.3°C</td>
<td>34.3°C</td>
</tr>
</tbody>
</table>
The results show the conservative conception of the core losses model adopted, once that in both cases the measured temperature rise were less than the estimated values. Considering the temperature rise calculation method, which is based in the empirical equation (7), and the complexity that the real environment indeed present, the experimental results indicate that the adopted model can be useful to find the pair: switching frequency and input current ripple that minimizes the boost inductor volume in the PFC boost converters.

VI. CONCLUSION

Concerning the single-phase PFC boost converter, this paper investigates the dependence of the magnetic volume with the switching frequency and input current ripple amplitude, considering the compliance with IEC 61000-3-2 and CISPR 22 standards. In the carried out analysis is considered a toroidal powder core with a single layer winding layout for implementation of the boost inductor. Taking into account constraints such as power density, leakage capacitances, irradiated noise and costs, this arrangement has been shown as a suitable choice for this application.

The main limiting factors for both switching frequency and input current ripple elevation were considered: the conduction losses, the core temperature rise and the DM noise generation. Regarding these restrictions, it was suggested a method to define an appropriate selection of the pair: input current ripple amplitude and switching frequency, aiming to minimize the boost inductor volume. All the models utilized on the proposed algorithm already were tested and confirmed in the literature.

The simulation and the experimental results validate the proposed algorithm and the performed analysis, which show that a proper combination of the switching frequency and input current ripple amplitude can leads to obtain a magnetic volume reduction. For example, comparing the typical suggested ripple amplitudes of 20% [17] with the achieved results, a volume reduction of 63% is obtained, by only pushing the ripple amplitude from 20% to 70% in the 46.6kHz curve, as indicate Figure 5. Even so, the single stage EMI input filter keeps able to provide enough attenuation in the DM noise to comply the converter with the EMI standard.

The use of the developed simulation algorithm contributes to achieve higher power densities and costs reduction of the CCM PFC boost converter through an adequate design of the main magnetic element.

ACKNOWLEDGEMENT

The authors would like to express their gratitude to "Conselho Nacional de Desenvolvimento Científico e Tecnológico – CNPq" (proc. 200049/2005-4). The authors would like to thank Profs. J. Sebastian, A. Fernández, M. M. Hernando and D. G. Lamar for their help and valuable discussions during the post-doctoral stage of Prof. H. L. Hey (grant from CNPq) in Universidad de Oviedo-Spain.

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